AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for erasing a block of memory in a flash memory device, the block of memory having a plurality of memory cells organized in columns and rows, the method comprising:

generating an erase pulse to the block of memory without performing a prior preprogram step;

performing a current leakage check on each column;

if a column is detected having current leakage, determining an overerased memory cell in the column that has an erase current greater than a first reference current level; and

applying a soft program pulse to the overerased memory cell until the erase current is less than the first reference current level.

2. (Original) The method of claim 1 and further including, prior to performing the current leakage check, applying additional erase pulses to memory cells that have an erase current less than a second reference current level until the erase current is at least equivalent to the second reference current level.

3. (Original) The method of claim 2 wherein the first and second reference current levels are sense amplifier reference current levels.

4. (Original) The method of claim 1 wherein the block of memory further includes a plurality of wordlines coupling rows of memory cells and the method further including applying a positive voltage to a selected wordline of the plurality of wordlines and a negative voltage to unselected wordlines.

5. (currently amended) The method of claim 1 wherein the soft program pulse is applied to the overerased memory cell until a first of the erase current reaches the is less than a second reference current level or a maximum quantity of soft program pulses is reached.

6. (Original) The method of claim 2 wherein the additional erase pulses are applied to memory cells having the erase current less than the second reference current level until a first of

the erase current is equivalent to the second reference current level or a maximum quantity of erase pulses is reached.

7. (Original)   The method of claim 1 wherein the flash memory is a NOR-type flash memory.

8. (Original)   The method of claim 1 wherein the flash memory is a NAND-type flash memory.

9. (currently amended) A method for erasing a block of memory in a flash memory device, the block of memory having a plurality of memory cells organized in columns coupled by bitlines and rows coupled by wordlines, the method comprising:

generating an erase pulse to the block of memory <u>without performing a prior preprogram step</u>;

performing a first erase verification on the block of memory to determine if each of the plurality of memory cells has an erase current less than a first reference current level;

performing a current leakage check on each column;

if a first column is detected having current leakage, performing a second erase verification to find an overerased memory cell in the first column; and

applying a soft program pulse to the overerased memory cell until an erase current of the overerased memory cell is less than ~~the~~ <u>a</u> second reference current level or a maximum quantity of soft program pulses are applied.

10. (Original) The method of claim 9 wherein the second erase verification begins at the first column.

11. (Original) The method of claim 9 wherein the soft program pulses are applied until the erase current is substantially equivalent to the second reference current level.

12. (Original) A method for erasing a block of memory in a flash memory device, the block of memory having a plurality of memory cells organized in columns coupled by bitlines and rows coupled by wordlines, the method comprising:

generating an erase pulse to the block of memory;

performing a first erase verification on the block of memory to determine if each of the

plurality of memory cells has an erase current less than a first reference current

level;

applying additional erase pulses to any memory cell of the plurality of memory cells

having an erase current less than the first reference current level until either the

erase current is substantially equal to or greater than the first reference current

level or a maximum quantity of additional erase pulses is applied;

performing a current leakage check on each column;

if a column is detected having current leakage, performing a second erase verification to

find in the column an overerased memory cell having an erase current

substantially equal to or greater than a second reference current level; and

applying a soft program pulse to the overerased memory cell until either the erase current

of the overerased memory cell is less than the second reference current level or a

maximum quantity of soft program pulses are applied.

13. (Original) The method of claim 12 and further including indicating an erase error when

either the maximum quantity of additional erase pulses or the maximum quantity of soft

program pulses is applied.

14. (Original) The method of claim 12 and further including:

applying a positive voltage to the wordlines of the block of memory; and

applying a negative voltage to unselected wordlines of the block of memory.

15. (Original) The method of claim 12 wherein voltages used in the soft program pulse are less

than voltages used in a program pulse.

16. (currently amended) A flash memory device comprising:

a block of memory comprising a plurality of memory cells arranged in rows and columns

such that the rows are coupled with wordlines and the columns are coupled with

bitlines; and

a control circuit that executes methods including generating an erase pulse to the block of

memory without performing a prior preprogram step, performing a current

leakage check on each column, if a column is detected having current leakage,

determining an overerased memory cell in the column that has an erase current greater than a first reference current level, and applying a soft program pulse to the overerased memory cell until either the erase current is less than the first reference current level or a maximum quantity of soft program pulses are applied.

17. (Original) The flash memory device of claim 16 wherein the array of memory cells is a NOR architecture.

18. (Original) The flash memory device of claim 16 wherein the array of memory cells is a NAND architecture.

19. (Original) The flash memory device of claim 16 and the control circuit further executes methods including, prior to performing a current leakage check, performing an erase verification on the plurality of memory cells and applying additional erase pulses to any memory cells of the plurality of memory cells that have an erase current less than a second reference current level.

20. (currently amended) An electronic system comprising:

a processor that generates control signals; and

a flash memory device, coupled to the processor, that accepts the control signals and stores data in a plurality of memory cells, the device comprising:

an array of memory cells arranged in rows and columns such that the rows are coupled with wordlines and the columns are coupled with bitlines; and

a control circuit that executes methods including generating an erase pulse to the block of memory without performing a prior preprogram step, performing a current leakage check on each column, if a column is detected having current leakage, determining an overerased memory cell in the column that has an erase current greater than a first reference current level, and applying a soft program pulse to the overerased memory cell until either the erase current is less than the second reference current level or a maximum quantity of soft program pulses are applied.

21. (Original) The system of claim 20 wherein the control circuit is a state machine.

22. (Original) A method for erasing a block of memory in a flash memory device, the block of memory having a plurality of memory cells organized in columns coupled by bitlines and rows coupled by wordlines, the method comprising:

generating an erase pulse to the block of memory;

performing a first erase verification on the block of memory to determine if each of the plurality of memory cells has an erase current less than or substantially equal to a first reference current level, wherein a selected wordline has a positive voltage applied and all unselected wordlines have a negative voltage applied;

performing a current leakage check on each column;

if a first column is detected having current leakage, performing a second erase verification to find an overerased memory cell in the first column, wherein a selected wordline has a positive voltage applied and all unselected wordlines have a negative voltage applied; and

applying a soft program pulse to the overerased memory cell until either an erase current of the overerased memory cell is less than the second reference current level or a maximum quantity of soft program pulses are applied.

23. (Original) The method of claim 22 wherein the positive voltage is substantially equal to 4.5V and the negative voltage is substantially equal to −1.5V.

24. (Original) The method of claim 22 wherein the maximum quantity of soft program pulses is substantially equal to one thousand.